IN THE SPECIFICATION:

After the Title of the Invention and before line 1, insert the following new heading and paragraph:

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a division of Application No. 10/147,417, filed on May 16, 2002, now U.S. Patent No. 6,757,875, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed.

Paragraph beginning at line 5 of page 1 has been amended as follows:

In fabricating a semiconductor device (hereafter, abbreviated simply as semiconductor fabrication), first, a pattern of a semiconductor is designed and the pattern is ~~memorized to store~~ stored as CAD data. Based thereon, a photomask is fabricated and the semiconductor element is not fabricated respectively as a single member thereof but a number of devices are simultaneously fabricated on one ~~sheet of a~~ semiconductor wafer. Therefore, the photomask is drawn with patterns of a number the same as that of devices fabricated on the one ~~sheet of~~ semiconductor wafer. However, ~~, however,~~ when the wafer is printed by the mask simply aligned with the same images, the ~~completely same~~ identical

circuit pattern is not photographed at a central portion and a peripheral portion of the wafer. This is because warp is necessarily accompanied by ~~being influenced by~~ the influence of aberration or ~~the~~ like errors of an optical system. Therefore, according to a circuit pattern, there is designed a pattern ~~taking~~ having a margin anticipating a safety factor in consideration of the aberration of the optical system actually used in transcription such that the circuit ~~constitution~~ becomes normal throughout ~~in all the area on~~ the transcribed wafer. The transcription of the pattern is executed not only for a single layer, but a plurality of ~~by being~~ overlapped ~~over a number of~~ layers in a thickness direction of the wafer. Further, patterns of different layers are formed by being transcribed by different masks and a circuit is constituted for an individual device and therefore, there is needed a connection among the patterns of the different layers. Therefore, shapes of the patterns among the different masks and positional relationship thereof constitutes an important yield factor in fabricating the semiconductor device. Further, as described above, a number of the devices are formed on the wafer and it is necessary that the shapes of the respective patterns and the positional relationship thereamong, are converged in an allowable range (within margin) of the design standard both at the central portion and

the peripheral portion. Particularly, since the large amount of semiconductors are fabricated based on the mask and therefore, finishing accuracy thereof is an important item directly influencing on the yield of the product.

Paragraph beginning at line 14 of page 3 has been amended as follows:

The present invention relates to an apparatus ~~of~~ for evaluating a layer matching deviation which is ~~having a function~~ capable of determining whether a pattern of a semiconductor device falls in ~~a~~ an allowable range of design including a relative positional relationship with a pattern of a later step to be able to carry out instruction to improve yield at an early stage ~~of steps~~ of fabricating a semiconductor device.

Paragraph beginning at line 21 of page 3 has been amended as follows:

An apparatus ~~of~~ for evaluating a layer matching deviation based on CAD information of the present ~~invention,~~ invention is provided with means for storing CAD data and a function of displaying an overlapped image of ~~to overlap~~ a scanning microscope image of a pattern of a semiconductor device formed on a wafer and a ~~design~~ CAD image used to

fabricate the device read from the storing means and a function of evaluating acceptability of formation of the pattern by displaying an overlapped image of ~~to overlap~~ a pattern image of the semiconductor device formed on the wafer and the ~~design~~ CAD image of the pattern, and, in addition thereto, ~~a function~~ is capable of evaluating acceptability of formation of the pattern also with regard to a shape and positional relationship with a pattern to be formed at a later step by displaying an overlapped image of ~~to overlap~~ a ~~design~~ CAD image of the pattern to be formed at the later step.

Paragraph beginning at line 17 of page 5 has been amended as follows:

According to an apparatus of observing a wafer pattern for evaluating acceptability of forming a pattern, there is observed a portion of a pattern constituting an observation object disposed within an area of about several through several ~~tens .~~ tens square of microns in a pattern formed on a wafer by enlarging the portion with high magnification and therefore, it is necessary to highly accurately position an observation field of vision of the wafer pattern observing apparatus to a desired observation position on a wafer pattern. Hence, conventionally, as a navigation method for the positioning, there is generally used

so-to-speak CAD navigation for specifying the observation object by using a CAD apparatus and by development of a semiconductor fabricating technology in recent years, a dimension of a pattern formed on a wafer becomes a submicron order and in order to observe such an ultra fine pattern, there has been used a wafer pattern observing apparatus having a high magnification of a multiplication factor of several tens of thousands.

Paragraph beginning at line 11 of page 6 has been amended as follows:

According to the invention, there is used a wafer pattern observing apparatus having the CAD navigation function, the apparatus ~~is~~ being provided with a function of displaying in an overlapped manner ~~to overlap~~ a scanning microscope image of a pattern of a semiconductor device formed on the wafer and a design CAD image read from storing means, wherein the apparatus is not only provided with a function of evaluating acceptability of forming the pattern by displaying ~~to overlap a~~ the overlapped pattern image of the semiconductor device formed on the wafer and the design CAD image of the pattern, but also a function capable of reading a design CAD image of a pattern formed at a later step by sampling the design CAD image from the storing means and displaying the

design CAD image to overlap the current microscope image, thereby, there can be checked and evaluated also a shape and positional relationship of ~~the~~ a ~~formed current~~ currently formed pattern and ~~the~~ a pattern to be formed in ~~the~~ a later step. The invention is characterized in that not only it is possible to check ~~checked~~ whether ~~the~~ a pattern which has already been formed falls in an allowable range of the design pattern but also the shape and positional relationship with ~~the~~ a pattern to be formed at ~~the~~ a later step can be checked in advance ~~previously~~. By enabling ~~to grasp~~ a shape defect to be detected at an early ~~time~~ point in time, occurrence of a failure thereafter can be prevented beforehand by feeding back improvement ~~instruction~~ instructions to a step of forming ~~an aimed~~ a desired pattern. Further, information of the shape defect ~~provided at the time point~~ can be reflected to promotion of yield of a product by feeding forward the information in the form of correcting the position of the pattern in the later step or the like to thereby correct the pattern and can also be reflected to a change in the design of the mask pattern per se. All of the countermeasures contribute to promotion of the yield of the device.

Paragraph beginning at line 16 of page 7 has been amended as follows:

Fig. 1A shows an image of a microscope having high magnification specifying a certain pattern in one chip on a wafer and Fig. 1B shows a CAD image of the pattern. Fig. 1C shows the two images ~~to overlap~~ overlapped on a display. Numeral 21 denotes a SEM image of a first metal layer, 22 denotes a CAD image of a first metal layer, 23 denotes an overlapped image of a CAD image and a SEM image. It is found that the pattern image observed in the example matches excellently with the design CAD image although only corner portions thereof are rounded. Further, the phenomenon of rounding the corner portions is a well-known phenomenon in the field of photolithography and the deformation is anticipated from the start. Now, it has been found that the pattern formed in the observation is constituted by a proper shape matching with the CAD image and it is observed by an image shown in Figs. 2A-2B whether the pattern is proper also in a relationship with a pattern formed in a later step. Numeral 24 denotes a CAD image of a second metal layer, 25 denotes a via layer. Fig. 2A is a CAD image displaying to overlap the pattern to be formed in a successive step and thereafter to an aimed pattern and Fig. 2B shows an image displaying the CAD image of Fig. 2A on a display to overlap onto a formed pattern at a current time point. The pattern adopted in Figs. 1A-1C and Figs. 2A-2B, is designed such that a second rectangular

metal layer is formed above a metal layer in an L-like shape and a via layer for shortcircuiting the two patterns is formed at end portions of the two metal layers. When observed by Fig. 2B, the CAD image of the second material layer of the later step, overlaps the first metal layer 23 which has already been formed and also a CAD image of the via layer 25 for shortcircuiting the two metal layers is positioned at the area overlapping the two metal layers. It is found that formation of the first metal layer 23 is proper also in the positional relationship with the pattern at the later step.

Paragraph beginning at line 22 of page 9 has been amended as follows:

Next, an explanation will be given of an embodiment and a processing flow of the invention ~~in~~ with reference to Fig. 4. Fig. 4 is a block diagram showing a basic ~~constitution~~ layout of an apparatus used in practicing the invention and numeral 1 designates a navigation apparatus for specifying an observation field of vision of a desired position. As the navigation apparatus 1, there is used ~~a~~ ~~constitution~~ an apparatus presented in Japanese Patent Application No. 2000-214846, entitled "Navigation method and apparatus for observing pattern of semiconductor apparatus", which ~~has been~~ was filed previously by the inventors and is

incorporated herein by reference. The ~~, that is, a~~ navigation apparatus comprises ~~"comprising~~ designating means for designating a predetermined portion, memory means for storing CAD data in correspondence with a pattern, low magnification pattern image data acquiring means for acquiring low magnification pattern image data of a semiconductor device by matching an observation position of the pattern observing apparatus by low magnification to make a center of observation of the predetermined portion fall in an observation field of vision in response to the designating means, means for outputting edge line segment data by sampling an edge of the pattern based on the low magnification pattern image data, means for providing CAD line segment data in correspondence with the low magnification pattern image data in response to the designating means and the memory means, means for calculating a deviation amount between the center of observation and a center of the observation field of vision by comparing the CAD line segment data and the edge line segment data, and means for executing a position control such that the center of observation and the center of the observation field of vision coincide with each other by compensating for a stage error of a stage based on the deviation amount" in order to observe by enlarging the predetermined portion of the pattern of the semiconductor device set to the stage by the pattern observing apparatus while enlarging in a high magnification.